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H4L LECTP

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(54) Abstract Title
Method of reducing energy consumption in a mobile transceiver

(57) A method for reducing energy consumption in a digital communication system in idle mode includes the steps of: estimating a received signal quality value (80) prior to decoding of the received message packet; skipping the convolutional decoding and instead hard sample-to-bit converting (82) of the samples when received signal quality value is within a predetermined valid range, thereby producing a plurality of estimated bits; decoding the estimated bits by utilizing predetermined decoding data, when received signal quality is outside a predetermined valid range, thereby producing decoded bits. The higher power-consuming convolutional decoding is thereby avoided in favour of lower power hard sample-to-bit converting when the received signal is of sufficiently high quality.

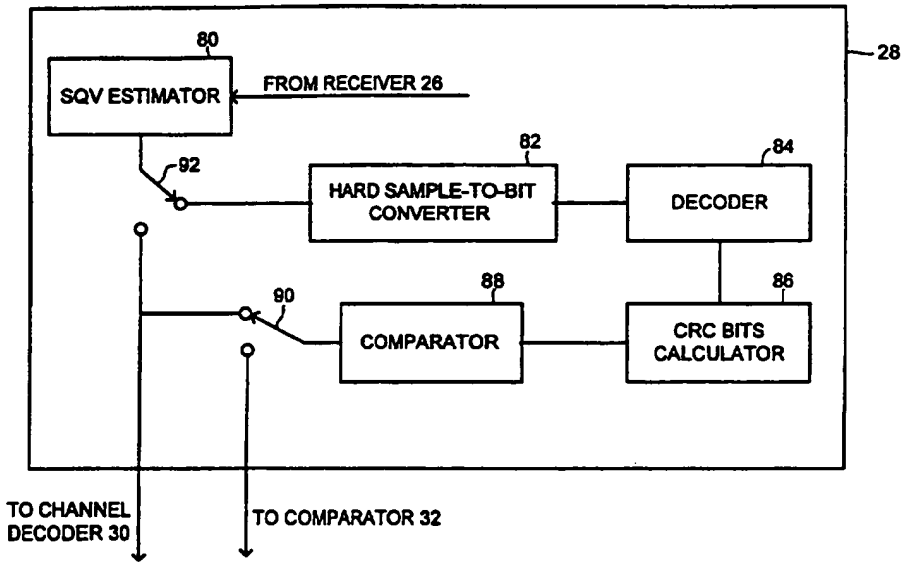

FIG. 3

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

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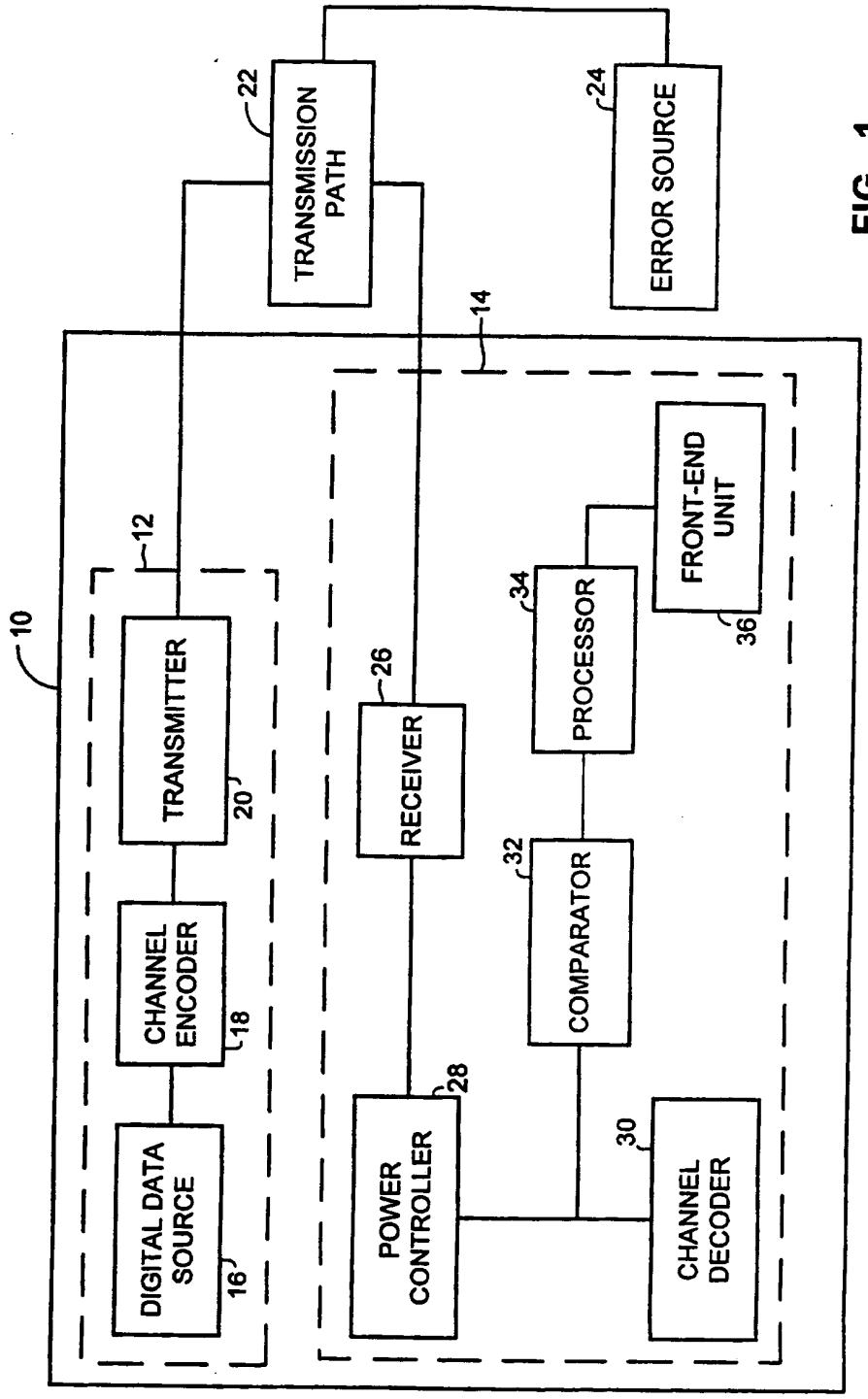
10
12
TRANSMITTER
20
CHANNEL ENCODER
18
DIGITAL DATA SOURCE
16
22
TRANSMISSION PATH
24
ERROR SOURCE
14
26
RECEIVER
28
POWER CONTROLLER
34
PROCESSOR
32
COMPARATOR
30
CHANNEL DECODER
FRONT-END UNIT
36

FIG. 1

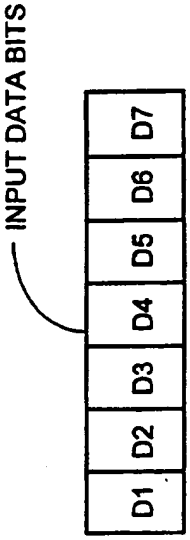

FIG. 2A

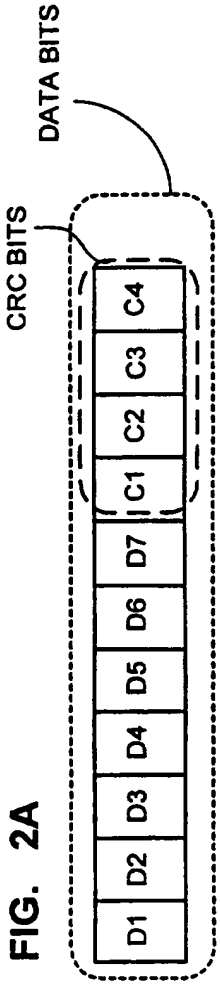

FIG. 2B

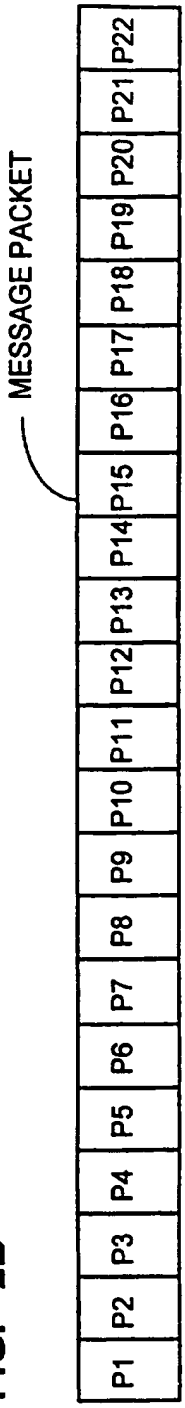

FIG. 2C

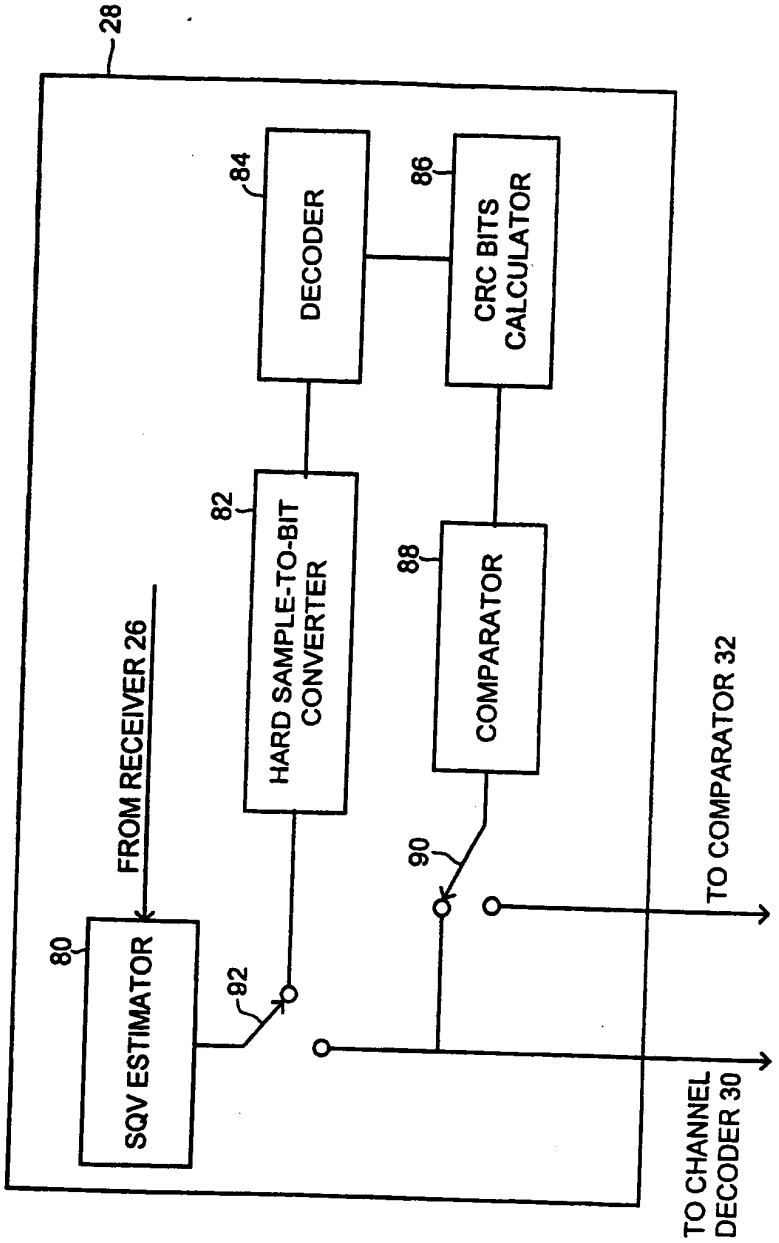
28
84
DECODER
86
CRC BITS CALCULATOR
82
HARD SAMPLE-TO-BIT CONVERTER
88
COMPARATOR
FROM RECEIVER 26
80
SQV ESTIMATOR
82
90
TO COMPARATOR 32
TO CHANNEL DECODER 30

FIG. 3

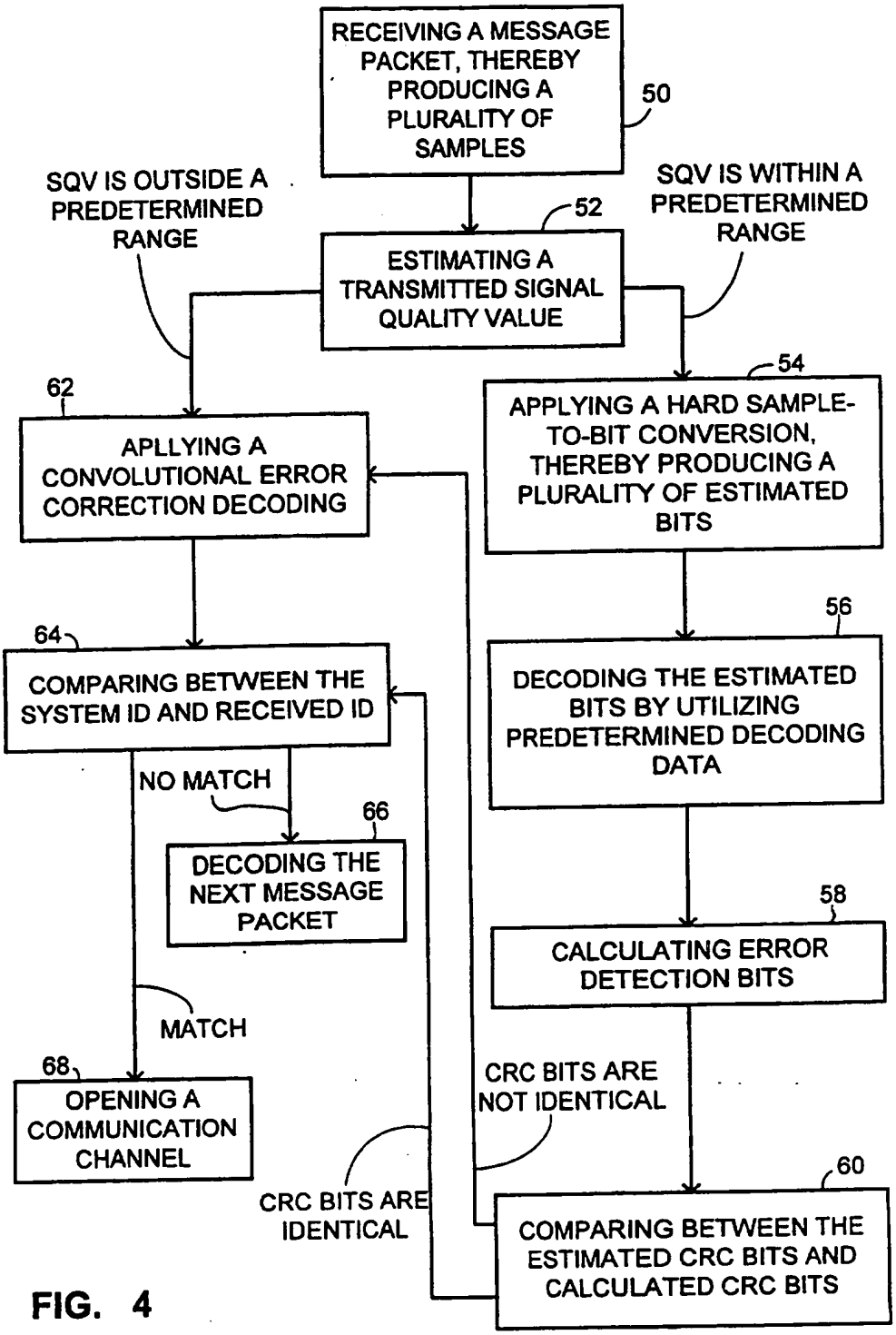
RECEIVING A MESSAGE PACKET, THEREBY PRODUCING A PLURALITY OF SAMPLES
50
ESTIMATING A TRANSMITTED SIGNAL QUALITY VALUE
52
SQV IS OUTSIDE A PREDETERMINED RANGE
SQV IS WITHIN A PREDETERMINED RANGE
APPLYING A HARD SAMPLE-TO-BIT CONVERSION, THEREBY PRODUCING A PLURALITY OF ESTIMATED BITS
54
APLLYING A CONVOLUTIONAL ERROR CORRECTION DECODING
62
DECODING THE ESTIMATED BITS BY UTILIZING PREDETERMINED DECODING DATA
56
COMPARING BETWEEN THE SYSTEM ID AND RECEIVED ID
64
NO MATCH
DECODING THE NEXT MESSAGE PACKET
66
CALCULATING ERROR DETECTION BITS
58
MATCH
OPENING A COMMUNICATION CHANNEL
68
CRC BITS ARE NOT IDENTICAL
CRC BITS ARE IDENTICAL
COMPARING BETWEEN THE ESTIMATED CRC BITS AND CALCULATED CRC BITS
60

FIG. 4

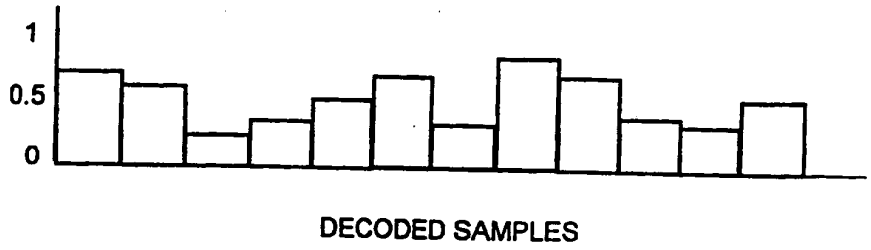

FIG. 5A

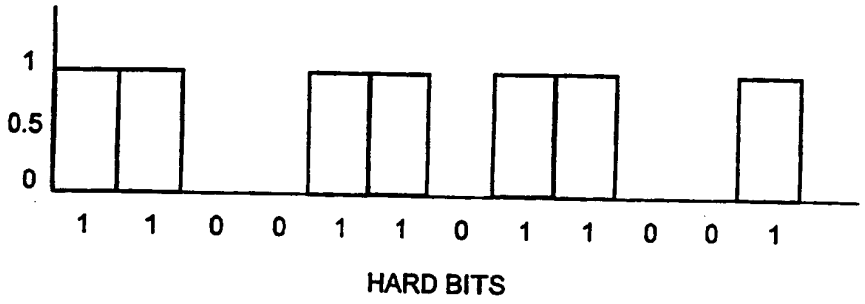

FIG. 5B

METHOD AND SYSTEM FOR REDUCING POWER CONSUMPTION IN COMMUNICATION DEVICES

FIELD OF THE INVENTION

The present invention relates to digital communication systems in general, and to methods and systems for minimizing energy consumption during stand-by (idle) operation mode of mobile communication systems, in particular.

BACKGROUND OF THE INVENTION

A typical cellular telephone system includes a plurality of base stations, each serving a pre-assigned geographical cell or region. Each base station transmits messages to a multitude of mobile units in its region. Each mobile unit includes microprocessor-controlled transceiver and decoder.

To initiate communication with the mobile units, a base station transmits a control message via a control channel. All of the mobile units, which are in stand-by mode of operation (idle mode), detect signals received via the control channel. A message, which is intended for a specific mobile unit, contains a representation of the unique identification code of that mobile unit.

A mobile unit, detecting a message via the control channel, analyzes the embedded identification code and compares it with its own identification code. In case both identification codes are identical, the mobile unit typically shifts to a particular communication channel whereupon the mobile unit can transmit and receive voice and/or data information on the particular channel, which has been assigned to it.

Many messages are transmitted by a respective base station and, of all those many messages, only a very small amount, if any, are intended for a particular mobile unit. Nevertheless, during the stand-by mode of operation, each mobile unit continuously receives and decodes all messages transmitted by the respective base station.

Conventional mobile units consume electrical power in both the talk and the stand-by modes. In current portable battery-operated mobile units, a major electrical current consumer is the receiver section of the transceiver. As previously described, the receiver section is continuously on, while the telephone is waiting to decode its identification code. The microprocessor and other electronic components on-board the mobile unit also consume the power during the stand-by mode and additionally contribute to current drain on the battery.

Methods and devices for reducing power consumption of mobile communication devices are known in the art. The conventional

approaches are: switching off all hardware components, which are not necessary at a predetermined time, using special "low-drain" modes of controllers and digital signal processors, these modes being entered whenever processors do not have a task to execute, using processors not at the highest clock speed, skipping some of receive slots while in an idle mode, and the like.

SUMMARY OF THE PRESENT INVENTION

It is an object of the present invention to provide a novel method and system for reducing energy consumption in mobile communication systems, which overcome the disadvantages of the prior art.

In accordance with the present invention, there is thus provided a device for reducing energy consumption in a digital communication system. The digital communication system includes a receiver for receiving a plurality of data bits, which are convolutionally encoded in a message packet, and a channel decoder for decoding the message packet, thereby producing a plurality of samples. The device includes a signal quality estimator, connected to the receiver, a hard sample-to-bit converter, connected to the quality estimator and a decoder, connected to the hard sample-to-bit converter.

The signal quality estimator determines a received signal quality value from the samples. In the case when the received signal quality value is within a predetermined valid range, the hard sample-to-bit converter converts the samples into hard bits by employing predetermined decoding data, thereby producing decoded bits. The decoded bits include estimated input data bits and estimated error detection bits, while estimated input data bits include received identification code. The predetermined decoding data can be in the form of a decoding matrix or in the form of a look-up table. In case the received signal quality value is outside the

predetermined valid range, the channel decoder convolutionally decodes the samples, thereby producing an estimation of the input data bits.

The device further includes an error detection bits calculator, connected to the decoder, and a first comparator, connected to the error detection bits calculator. The error detection bits calculator calculates error detection bits from the estimated input data bits. The comparator compares between the calculated error detection bits and estimated error detection bits. In case the calculated error detection bits and estimated error detection bits are not identical, the channel decoder convolutionally decodes the samples.

The device can further include a second comparator, connected to the first comparator and to the channel decoder. The second comparator compares between the system ID and received ID and produces a corresponding control signal for operating the system. The control signal switches the system to a sleep mode for a predetermined time interval, if the system ID and received ID are not identical, and opens a communication channel, if system ID and received ID are identical.

In accordance with another aspect of the present invention, there is thus provided a method of reducing energy consumption in a digital communication system being in idle mode of operation. The system receives a message packet, consisting of a plurality of convolutionally

encoded data bits and processes the message signal, thereby producing a plurality of samples. The system utilizes a convolutional decoding procedure for extracting the data bits from the samples. The method of reducing energy consumption includes the steps of:

- estimating a received signal quality value, prior to decoding of the received message packet,
- skipping the convolutional decoding and hard sample-to-bit converting of the samples, when received signal quality value is within a predetermined valid range, thereby producing a plurality of estimated bits, and,
- decoding the estimated bits by utilizing predetermined decoding data, when received signal quality is outside a predetermined valid range, thereby producing decoded bits.

The decoded bits include estimated input data bits and estimated error detection bits. The predetermined decoding data can be in the form of a decoding matrix or in the form of a look-up table. The convolutional decoding procedure for extracting the data bits from the samples can include a sequential maximum likelihood sequence estimation prediction of the received message packet.

The method can further include the steps of: calculating error detection bits corresponding to the input data bits, and comparing between the estimated error detection bits and calculated error detection bits. The method can further include the steps of:

- comparing between a digital communication system identification code and a received identification code, when the estimated error detection bits and the calculated error detection bits are identical, wherein the received identification code is embedded in the input data bits,
- convolutionally decoding the received message packet when the estimated error detection bits and the calculated error detection bits are not identical, and
- comparing between the system ID and received ID.

The method further includes the steps of: opening a communication channel when the system ID and received ID are identical, shutting down the system for a predetermined time interval when the system ID and received ID are not identical, and, repeating operation from estimating the quality of the received signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

Figure 1 is a schematic illustration of a communication system, constructed and operative in accordance with a preferred embodiment of the present invention,

Figure 2 is an exemplary illustration of the data structure used in the preferred embodiment of the present invention,

Figure 3 is a schematic illustration in detail of a power controller, constructed and operative in accordance with a further preferred embodiment of the present invention,

Figure 4 is a schematic illustration of a method for operating a power controller, operative in accordance with a further preferred embodiment of the present invention, and

Figure 5 is an exemplary schematic illustration of conversion of demodulated samples into hard bits in case of a binary modulation scheme.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention overcomes the disadvantages of the prior art by providing a novel method and device for reducing power consumption in digital communication systems by replacing a conventional convolutional decoding during the error correction phase by a simpler and faster procedure.

Reference is now made to Figure 1, which is a schematic illustration of a communication system, generally referenced 10, constructed and operative in accordance with a preferred embodiment of the present invention. System 10 includes a transmitting unit 12 and a receiver unit 14. Transmitting unit 12 includes a digital data source 16, a channel encoder 18 and a transmitter 20. Channel encoder 18 is connected to digital data source 16 and to transmitter 20.

Receiver unit 14 includes a receiver 26, a power controller 28, a channel decoder 30, a comparator 32, a processor 34 and a front-end unit 36. Power controller 28 is connected to receiver 26, to channel decoder 30 and to comparator 32. Comparator 32 is connected to power controller 28, to channel decoder 30 and to processor 34. Processor 34 is connected to front-end unit 36.

Digital data source 16 provides data to channel encoder 18. At every time instance, channel encoder 18 processes a predetermined

number of the input data bits. Channel encoder 18 adds error detection bits to the input data bits and encodes the resulting data, also called a "data packet", into a "message packet". The message packet contains both an error detection and error correction information, which can be used by the receiving end of the system to detect and to correct errors.

An example for a conventional method for producing correction information is convolutional forward error correction (FEC) coding. In this technique the channel encoder 18 determines a set of parity bits, based on the data packet bits. For each bit of the L bits of a data packet, channel encoder 18 generates r parity bits, which are packed into a message packet, for transmission to the receiving end. The rate of the code is defined as a ratio of the number of input data bits to the number of parity bits. The parity bits can be calculated, for example, according to predetermined Boolean combinations of various bits of the data packet.

Cyclic Redundancy Check (CRC) method is an example of an error detection technique, which results in generating and adding error detection bits called "check", or "CRC bits", to the input data bits. The "check" bits are calculated based on the input data bits. The "check" bits constitute a "checkword" that is specific to a given input data bits. The checkword is appended to the input data, so that both are processed through the same channel encoder, both are transmitted through

transmission path together, and both are processed through the same decoder in the receiver.

It is noted that some communication systems include an internal CRC calculator, which can calculate "check" bits from the decoded message packet bits.

These receiver-calculated "check" bits are compared with the decoded "check" bits from the message packet. Any noncompliance therebetween indicates an error, and the degree of compliance (i.e., amount of error bits, statistical criteria and the like) can be used as a quantitative measure of the reliability of the data transmission.

Channel encoder 18 provides the message packets to transmitter 20. Transmitter 20 modulates the message packets with a carrier signal, amplifies the modulated signal and transmits it. The transmitted signal travels though transmission path 22, which is typically wireless, and normally introduces errors (designated by error source 24) into the transmitted signal. Receiver 26 receives the signal, transmitted via transmission path 22, demodulates it and provides the demodulated signal, which is a set of samples, to power controller 28.

According to the present invention, power controller 28 estimates a signal quality value (SQV) of the received signal, and uses the result to select a method of error correction and error detection,

accordingly. It is noted that SQV can be a set of criteria, including the amplitude of the signal, statistical characteristics of the signal and the like. When the estimated SQV is outside a predetermined high quality range, then the power controller 28 provides the received signal to channel decoder 30. Channel decoder 30 performs conventional decoding, error correction and detection procedure (e.g., Viterbi trellis and the like) on the received signal. When the estimated SQV is within the predetermined valid range, then power controller 28 utilizes a simplified low processing decoding, which will be disclosed in detail hereinafter. The output of power controller 28 is either a decoded signal, which includes a received identification code, or a control signal for channel decoder 30 to decode the received signal.

Comparator 32 receives a decoded signal from either power controller 28 or channel decoder 30. Comparator 32 compares between the received identification code (received ID) and a system identification code (system ID), which is the identifying number of the receiver unit 14. Comparator 32 generates a control signal as a result of comparison, and provides it to processor 34. Receiver unit 14, depending on the control signal value, either enters a sleep mode for a predetermined time interval, or opens a channel for communication via front-end unit 36. It is noted that

sleep mode is characterized by shutting down most of the activities of the receiving station 14.

Reference is now made to Figure 2, which is an exemplary illustration of the data structure used in the preferred embodiment of the present invention (Figure 1). Figure 2A represents input data, which consists of L=7 bits *D1...D7*. After addition of M=4 "check" bits, the data packet consists of $L+M$ bits *D1...D7,C1...C4* (Figure2B), which are an input for an encoding procedure. Figure 2C represents a message packet, which is rate 1/2 encoded data packet. Two parity bits are calculated, for each bit of the $L+M$ bits of the input data packet, so that a total of $2*(L+M)$ bits *P1... P22* are generated.

Reference is now made to Figure 3, which is a schematic illustration in detail of power controller 28 (Figure 1), constructed and operative in accordance with a further preferred embodiment of the present invention. Power controller 28 includes a SQV estimator 80, a hard sample-to-bit converter 82, a decoder 84, a CRC bits calculator 86, a comparator 88 and two switches 90 and 92. SQV estimator 80 is connected to switch 92. Hard sample-to-bit converter 82 is connected to switch 92 and to decoder 84. CRC bits calculator 86 is connected to decoder 84 and to comparator 88. Switch 90 is connected to comparator 88. Switch 92 is operative to connect SQV estimator 80 with either hard

sample-to-bit converter 82 or with channel decoder 30 (Figure 1). Switch 90 is operative to connect comparator 88 with either channel decoder 30 or with comparator 32 (Figure 1). SQV estimator 80 receives signal samples from receiver 12 (Figure 1), and estimates an SQV. When the estimated SQV is outside a predetermined valid range, then, SQV estimator 80 activates switch 92 to connect to channel decoder 30 (Figure 1). SQV estimator 80 further provides the signal samples to channel decoder 30 (Figure 1). Channel decoder 30 (Figure 1) decodes the received signal using one of the conventional convolutional decoding procedures, which are known in the art.

When the estimated SQV is within a predetermined valid range, then SQV estimator 80 activates switch 92 to connect to hard sample-to-bit converter 82. SQV estimator 80 further provides the signal samples to hard sample-to-bit converter 82. Hard sample-to-bit converter 82 converts samples into bits and provides them to decoder 84. Decoder 84 decodes the received bits, using low processing procedure, and provides decoded signal, which is an estimation of input data bits and CRC bits, to CRC bits calculator 86. CRC bits calculator 86 calculates CRC bits from the estimated input data bits and provides the result of calculation to comparator 88. Comparator 88 compares between the calculated CRC bits and the received CRC bits and generates a control signal thereof.

Comparator 88, depending on a comparison result, activates switch 90 to connect to channel decoder 30 or to comparator 32 (Figure 1).

Reference is further made to Figure 4, which is a schematic illustration of a method for operating power controller 28 (Figure 1), operative in accordance with a further preferred embodiment of the present invention. In step 50 a message packet is received. With reference to Figure 1, receiver 26 receives the message packet, thereby producing a plurality of signal samples. In step 52, an SQV is estimated. With reference to Figure 1, power controller 28 receives signal samples from receiver 26 and determines the SQV. If the SQV is outside a predetermined range (low quality), then the system proceeds to step 62 and performs conventional convolutional decoding, error correction and detection. Any conventional method for decoding convolutional codes, can be used, such as, for example, the method described in the article by D. Forney, "The Viterbi Algorithm", Proc. IEEE, vol.61, pp. 268-278 (Mar., 1973). A description of other decoding methods can be found in L. H. Charles Lee, "Convolutional Coding: Fundamentals and Applications", Artech House, Boston-London, 1997.

If the SQV is within the predetermined valid range (high quality), then it is assumed that the received signal is free of errors and thus, the system proceeds to step 54 and performs simplified, energy saving

decoding of the received signal, which will be described in detail hereinbelow.

In step 54, the received samples are converted into hard bits. With reference to Figure 3, hard sample-to-bit converter 82 receives signal samples from SQV estimator 80 via switch 92, and converts them into hard bits. The conversion can be performed based on the following criteria: each of the received samples having a value equal or greater than 0.5 (or any other predetermined threshold) is considered as bit "1", all other samples are considered as bits "0". It is noted, that the above is true only if each received symbol represents a single digital bit information (binary modulation). Generally, several bits are mapped into symbols by the transmission system (multi-level modulation). In this case each symbol is converted into *m* bits, using a hard decision with respect to particular modulation scheme.

Reference is now made to Figures 5A and 5B, which are an exemplary schematic illustration of the conversion of demodulated samples into hard bits in case of a binary modulation scheme. Figure 5A presents a demodulated set of samples, which are provided at the output of receiver 26. Part of these samples have the values equal to or greater than 0.5, and the rest have values less than 0.5. The output of the conversion procedure, accomplished according to the foregoing criteria, is

presented in Figure 5B. A new set of converted samples consists of hard bits, having values "0" or "1".

Referring back to Figure 4, step 56, the data bits are decoded. With reference to Figure 3, decoder 84 decodes the original encoded bits. Preferably, encoded input data and CRC bits are considered as the output of a block encoder. In this case the encoding process can be described by a predetermined matrix $\hat{R}$ of the form:

$$\hat{R} = \begin{bmatrix} xxxxxxx00.....00 \\ 0xxxxxxx00.....00 \\ 00xxxxxxx00.....00 \\ 000xxxxxxx00.....00 \\ ..... \\ ..... \\ 00.....0xxxxxxx0 \\ 00.....0xxxxxxx \end{bmatrix} \qquad (1)$$

In expression (1), every row of the encoding matrix $\hat{R}$ can be considered as a polynomial of the input data, which is shifted to the right by one index every next row. It is noted that the number of bits in each of the rows of the matrix $\hat{R}$ is set equal to 7 for exemplary purposes only. Considering original data together with CRC bits as a vector $\bar{X}$, and encoded bits as a vector $\bar{Y}$, we can write:

$$\bar{Y} = \hat{R} * \bar{X}. \qquad (2)$$

Consequently, the decoding process is expressed as:

$$\bar{X} = \hat{R}^{-1} * \bar{Y}, \qquad (3)$$

where $\hat{R}^{-1}$ denotes an inverse matrix.

Similar to matrix $\hat{R}$, matrix $\hat{R}^{-1}$ also has a single row pattern, which is shifted by one index every next row. The structure of the matrix $\hat{R}$ makes it possible to implement very fast algorithms, saving time and energy thereof. The output of the decoding operation is an estimation of the input data bits and CRC bits. It is noted that, matrix $\hat{R}$ can be replaced by a predetermined look-up table, or by any other appropriate type of decoding data structure.

In step 58, new CRC bits are calculated. With reference to Figure 3, CRC bits calculator 86 calculates CRC bits from the decoded input data bits.

In step 60, the calculated and received CRC bits are compared. With reference to Figure 3, comparator 88 compares between the calculated CRC bits and the decoded CRC bits. If both CRC sets are identical, then the received message packet is considered valid and receiver unit 14 proceeds to step 64. In the opposite case of non-identical sets of the CRC bits, receiver unit 14 proceeds to step 62, performs a set of procedures which include conventional convolutional decoding, error correction and error detection on received message packet, and proceeds to step 64. It is noted, however, that since the SQV is within the valid

range, then the probability for two CRC sets to be non-identical is very low.

In step 64, the system ID is compared with the received ID. With reference to Figure 1, comparator 32 compares between the system ID and the received ID. If these two IDs are not identical (no match), then the receiver unit 14 (Figure 1) switches to a sleep mode for a predetermined period of time, proceeds to step 66 and decodes the next message packet. If the system ID and received ID are identical (match), then the system proceeds to step 68 and processor 30 opens a channel for communication.

The above examples addressed a binary symbol encoding case, where an encoded data bit is identical to resulting symbol. It is noted that the method of the present invention can be adapted for use in communication standards, involving more advanced symbol encoding.

It will be appreciated by persons skilled in the art that the present invention is not limited to what has been particularly shown and described hereinabove. Rather the scope of the present invention is defined only by the claims, which follow.

CLAIMS

1. Method for reducing energy consumption in a digital communication system, the digital communication system being in idle mode, the digital communication system receiving a plurality of data bits, the data bits being convolutionally encoded in a message packet, the digital communication system processing the message packet, thereby producing a plurality of samples, the digital communication system utilizing a convolutional decoding procedure for extracting the data bits from the samples, the method comprising the steps of:

estimating a received signal quality value, prior to decoding said received message packet;

skipping said convolutional decoding, when said received signal quality value is within a predetermined valid range;

hard sample-to-bit converting said samples, when said received signal quality value is within a predetermined valid range, thereby producing a plurality of estimated bits; and

decoding said estimated bits by utilizing predetermined decoding data, when said received signal quality value is outside of a predetermined valid range, thereby producing decoded bits.

2. The method according to claim 1, wherein said decoded bits include estimated input data bits and estimated error detection bits.

3. The method according to claim 1, further comprising the steps of:

calculating error detection bits corresponding to said input data bits; and, comparing between said estimated error detection bits and said calculated error detection bits.

4. The method according to claim 3, further comprising the step of comparing between a digital communication system identification code and a received identification code, when said estimated error detection bits and said calculated error detection bits are identical, wherein said received identification code is embedded in said input data bits.

5. The method according to claim 3, further comprising the steps of:

convolutionally decoding said received message packet when said estimated error detection bits and said calculated error detection bits are not identical; and

comparing between said digital communication system identification code and said received identification code.

6. The method according to claim 5, further comprising the steps of:

shutting down the system for a predetermined time interval, when said digital communication system identification code and said received identification code are not identical; and

repeating from said step of estimating said received signal quality value.

7. The method according to claim 5, further comprising the step of:

opening a communication channel when said digital communication system identification code and said received identification code are identical.

8. The method according to claim 1, wherein said predetermined decoding data is in the form of a decoding matrix.

9. The method according to claim 1, wherein said predetermined decoding data is in the form of a look-up table.

10. The method according to claim 1, wherein said convolutional decoding procedure includes a sequential maximum likelihood sequence estimation prediction of said received message packet.

11. Device for reducing power consumption in a digital communication system (14), the digital communication system being in idle mode, the digital communication system including a receiver (26) for receiving a plurality of data bits, the data bits being convolutionally encoded in a message packet, the digital communication system including a channel decoder (30) for decoding the message packet, thereby producing a plurality of samples, the device comprising:

a signal quality estimator (80), connected to said receiver;

a hard sample-to-bit converter (82), connected to said signal quality estimator (80); and

a decoder (84), connected to said hard sample-to-bit converter (82).

12. The device according to claim 11,

wherein said signal quality estimator (80) determines a received signal quality value from said samples,

wherein said hard sample-to-bit converter (82) converts said samples into hard bits, when said received signal quality value is within a predetermined valid range,

said decoder (84) decodes said hard bits by employing predetermined decoding data, thereby producing decoded bits.

13. The device according to claim 12, wherein said decoded bits include estimated input data bits and estimated error detection bits.

14. The device according to claim 13, wherein said estimated input data bits include received identification code.

15. The device according to claim 12, further comprising an error detection bits calculator (86), connected to said decoder (84), wherein said error detection bits calculator (86) calculates error detection bits from estimated input data bits.

16. The device according to claim 15, further comprising a first comparator (88), connected to said error detection bits calculator (86), wherein said comparator (88) compares between said calculated error detection bits and said estimated error detection bits, thereby producing a control signal.

17. The device according to claim 12, wherein said predetermined decoding data is in the form of a decoding matrix.

18. The device according to claim 12, wherein said predetermined decoding data is in the form of a look-up table.

19. The device according to claim 12, wherein said channel decoder (30) convolutionally decodes said samples when said received signal quality value is outside a predetermined valid range, thereby producing an estimation of said input data bits.

20. The device according to claim 16, wherein said channel decoder (30) convolutionally decodes said samples, when said calculated error detection bits and said estimated error detection bits are not identical.

21. The device according to claim 11, further comprising a second comparator (32), connected to said first comparator (88) and to said channel decoder (30), wherein said second comparator compares between a digital communication system identification code and a received identification code, thereby producing a corresponding control signal for operating said digital communication system.

22. The device according to claim 21, wherein said corresponding control signal switches said digital communication system to a sleep mode,

for a predetermined time interval, when said digital communication system identification code and said received identification code are not identical.

23. The device according to claim 21, wherein said corresponding control signal opens a communication channel when said digital communication system identification code and said received identification code are identical.

24. The device according to claim 11, wherein said digital communication system is a mobile communication system.

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

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Other: Online: WPI, EDOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	WO 97/12491 A1 (PACIFIC)	
A	WO 92/09146 A1 (MOTOROLA)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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